

G H Ralsoni College of Engineering and Management, Pune.
 (An Autonomous Institution affiliated to Savitribai Phule ,Pune University)
FY B.TECH (TERM/SEM -I)
ESE WINTER 2024 (2023 Pattern)
Digital Logic Design (23UESL1105)

[Time:--2.30 hrs]

[Max. Marks 60]

Instructions to the candidates:

- 1) All questions compulsory.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.
- 5) Other Instructions, if any.

Q. No.	Sub Question	Marks	CO	BL
1	a) i) 1101.101 convert binary to decimal ii) (17CD) ₁₆ convert to octal.	[2] [2]	CO1 CO1	L2 L2
	b) Explain Excess-3 code. Convert given binary into gray code i)0110, ii)1101 , iii) 0111	[4]	CO1	L2
	c) Explain 1's compliment with example and perform subtraction of (8 - 5) using 2's compliment	[4]	CO1	L2
2	a) Reduce following function using K-map technique and Draw circuit using Logic gates. $F(A,B,C,D) = \sum_m (0,1,2,3,5,7,8,10,13,15)$	[6]	CO2	L4
	b) Implement full Subtractor using 8:1 MUX. Draw truth table and circuit Diagram.	[6]	CO2	L4
3	a) Explain shift register along with its types. Explain Right shift of bits in SISO shift register with circuit diagram.	[6]	CO2	L2
	OR			
	b) Design 2- bit Ripple /Asynchronous up counter. Explain in detail.	[6]	CO2	L4
	c) Explain working of T- flip-flop along with circuit diagram and truth table. State Applications of T-FF.	[6]	CO2	L2
4	a) Explain Moore model in detail.	[6]	CO3	L2
	OR			
	b) For the given sequence 1110, draw state diagram using Mealy model. Explain what State reduction is.	[6]	CO3	L4
	c) List the steps for designing FSM. Differentiate between mealy model and Moore model	[6]	CO3	L2
5	a) Explain in brief VHDL coding, its uses and syntax to write code.	[6]	CO4	L2
	b) Write VHDL code for Full Adder Using Dataflow Architecture.	[6]	CO4	L2