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G H Raisoni College of Engineering and Management, Pune.
(An Empowered Autonomous Institute affiliated to Savitribai Phule, Pune University, NAAC Accredited "A+" Grade)

FY B.TECH/(TERM II/SEM II)
ESE SUMMER 2025 (2023 Pattern)
Digital Logic Design (23UESL1105)

[Time: 2:30 Hours]

[Max. Marks 60]

Instructions to the candidates:

- 1) All questions compulsory.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.

Q.No.	Sub Question	Marks	CO	BL
1	a) i) $(10101)_2$ Convert the binary number to Decimal number ii) $(221)_8$ Convert Octal number to Decimal number iii) $(105)_{10}$ Convert Decimal to Binary number.	[6]	CO1	L2
	b) What is BCD Code? Explain in detail. Perform BCD addition of decimal numbers 2 & 6.	[6]	CO1	L2
	OR			
2	c) Enlist any two Boolean laws. State and prove De-Morgan's Theorems using truth table.	[6]	CO1	L2
	a) Reduced the following function using K-Map Techniques $F(A+B+C+D) = \pi M(0,3,4,7,8,10,12,14) + d(2,6)$	[6]	CO2	L2
3	b) Explain 4:1 multiplexer with proper circuit diagram. Implement the following Boolean function using 4:1 Mux. $F(ABC) = \sum m(1,3,5,6)$	[6]	CO2	L2
	a) Explain 4-bit Ring Counter with circuit diagram, truth table and waveforms.	[6]	CO2	L2
	b) Design 3-bit Ripple /Asynchronous up counter. Explain the working in detail.	[6]	CO2	L2
OR				
4	c) Explain shift register along with its types. Explain Right shift of bits in SISO shift register with circuit diagram.	[6]	CO2	L2
	a) List the steps for designing FSM. Differentiate between mealy model and Moore model	[6]	CO3	L2
5	b) For the given sequence 1001, draw state diagram using Mealy model with state table.	[6]	CO3	L2
	a) Elaborate with syntax Dataflow style, Behavior style, structure style of architecture in VHDL Programming.	[6]	CO4	L2
	b) Write VHDL code for half Subtractor Using Dataflow Architecture.	[6]	CO4	L2

NOTE:

- BL – Bloom's Taxonomy Levels (1- Remembering, 2- Understanding, 3 – Applying, 4 – Analyzing, Creating).

5 –Evaluating, 6 -