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G H Raisoni College of Engineering and Management, Pune

(An Empowered Autonomous Institute affiliated to Savitribai Phule, Pune University, NAAC Accredited "A+" Grade)

First Year B. Tech.

(TERM-I)

CAE II Winter 2025 (2023 Pattern)

Digital Logic Design(23UESL1105)

(Time: - 01 Hour) **(Max. Marks:20)**

Instructions to the students:

i) All questions are compulsory. ii) Neat diagrams must be drawn wherever necessary.
iii) Figures to the right indicate full marks. iv) Use of scientific calculator is allowed
v) Assume suitable data, if necessary.

Q.No	*Question*	Marks	CO	BL
1 a	Explain the term FSM briefly. Write the difference between the Melay Model and Moore Model	5	CO3	2
	OR			
1b	Describe Moore FSM with state diagram and state table.	5	CO3	2
1c	Design an FSM for serial sequence detector with the pattern 1101 with non-overlapping for Melay machine	5	CO3	3
	OR			
1d	Design sequence detector with the pattern 1001 with state diagram, state table using for Moore machine	5	CO3	3
2a	Describe VHDL. Explain Structure for VHDL program.	5	CO4	2
	OR			
2b	Explain the syntax Dataflow style, Behavior style, structure of architecture in VHDL programming	5	CO4	2
2c	Draw the block diagram, truth table, and write the VHDL code for 8:1 MUX using Behavioural modelling	5	CO4	3
	OR			
2d	Write the VHDL code for Full Adder and draw block diagram with truth table.	5	CO4	3

BL – Bloom's Taxonomy Levels (1- Remember, 2- Understand, 3 – Apply, 4 – Analyze,5 – Evaluate 6 - Create