

G H Raisoni College of Engineering and Management, Pune
(An Autonomous Institution affiliated to Savitribai Phule, Pune University)

Department of First Year B. Tech.

Term I (2024-25)

CAE-II

Subject Name: Digital Logic Design (23UESL1105)

[Time: 01 Hour]

[Max. Marks-20]

Instructions to the candidates:

- 1) All questions compulsory.
- 2) Neat diagrams must be drawn wherever necessary.
- 3) Figures to the right indicate full marks.
- 4) Assume suitable data, if necessary.
- 5) Other Instructions, if any.

Q. No.	Sub Question	CO	Marks	BL
1	a) Explain SR ff With truth table and what is the disadvantages of SR FF? how they can be avoided?	CO2	[5]	L1
	OR			
	b) What is race around condition in JK FF and how it can be avoided ?	CO2	[5]	L1
	c) Explain ring counter with waveform in detail?	CO2	[5]	L3
	OR			
	d) Explain 4 bit ripple up-counter with proper circuit diag?	CO2	[5]	L3
2#	a) What is shift register .What are various types of Shift Register ? Explain any one.	CO2	[5]	L4
	OR			
	b) Explain Mealy state machine with suitable block diagram.	CO3	[5]	L4
#	c) Explain Moore state machine with suitable block diagram	CO3	[5]	L2
	OR			
#	d) Difference between Mealy and Moore state machine.	CO3	[5]	L2