[Total No. of Ques.02] Seat No: [Total No. of Pages: 01]

G. H. Raisoni College of Engineering and Management, Pune.
(An Autonomous Institution affiliated to Savitribai Phule, Pune University)
F. Y. B.Tech. Department
CAE-1 : Term I(2024-25)
Digital Logic Design (23UESL1105)

[Time: 01 Hour] **[Max. Marks-20]**

Instructions to the candidates:
1) *All questions compulsory.*
2) *Neat diagrams must be drawn wherever necessary.*
3) *Figures to the right indicate full marks.*
4) *Assume suitable data, if necessary.*

Q.No.	Sub Question		CO	Marks	BL
Q.1	A)	Convert following numbers.	CO1	[5M]	L3
		i) Convert Binary to Decimal number. $(10101)_2$			
		ii) Convert Decimal to Binary number. $(105)_{10}$			
		iii) Convert Decimal to Hexadecimal number. $(122)_{10}$			
		iv) Convert Hexadecimal to Octal number. $(ABCD)_{16}$			
		v) State Any two ***Boolean Laws*** .			
	B)	State the De-Morgan's Theorems and verify using truth table.	CO1	[5M]	L3
		OR			
	C)	Perform subtraction using $2^{'s}$ complement method (15-7)	CO1	[5M]	L3
Q.2	A)	Explain Standard SOP form and Standard POS forms. Convert following equations into standard/ canonical SOP form, $f(A,B,C,) = (\bar{A}.C + \bar{A}.\bar{B}. + \bar{A}.\bar{B}.C)$	CO2	[5M]	L3
	B)	Solve the following equation using K-map, implement using Logic gates. $f(A,B,C,D) = \sum m(0,4,6,8,10,12,13) + d(2,14,15)$	CO2	[5M]	L4
		OR			
	C)	Design and implement Half Adder circuit using logic gates with K-map.	CO2	[5M]	L4