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G H Raisoni College of Engineering and Management, Pune

(An Empowered Autonomous Institute affiliated to Savitribai Phule, Pune University, NAAC Accredited "A+" Grade)

First Year B. Tech.

CAE I / Term II / AY 2025-26 (2023 Pattern)

Digital Logic Design (23UESL1105)

(Time: - 01 Hour) **(Max. Marks : 20)**

Instructions to the students:

i) All questions are compulsory.
ii) Calculator is allowed
iii) Figures to the right indicate full marks.

Question No		Marks	CO	BL
Q.1 a)	Convert the following Decimal number to Hexadecimal number $(445.27)_{10}$ $(122.75)_{10}$	5	CO1	L2
	OR			
Q.1 b)	What is Excess -3 code? Convert the decimal number $(48)_{10}$ into Excess-3 code. Convert binary number $(110101)_2$ to gray code.	5	CO1	L2
Q.1 c)	Reduce the following equation using Boolean Algebra theorems, and implement using logic gates. F(A,B,C)= A' B C + A' B' + A' B' C'	5	CO1	L2
	OR			
Q.1 d)	Perform the subtraction on following number using 1's compliment technique 1. $(23 - 13)_{10}$ 2. $(15-25)_{10}$	5	CO1	L2
Q.2 a)	What is flip-flop? How to design T FF from JK FF? Also write the application of T FF.	5	CO2	L2
	OR			
Q.2 b)	Convert the following function into standard POS form F(A,B,C)=(B + C) (A' + B') (A' + C')	5	CO2	L2
Q.2 c)	What is Multiplexer? Design 8:1 multiplexer using truth table and circuit diagram using logic gates.	5	CO2	L2
	OR			
Q.2 d)	Design Half Adder circuit. Draw logic diagram and truth table.	5	CO2	L2

BL – Bloom's Taxonomy Levels (1- Remember, 2- Understand, 3 – Apply, 4 – Analyze, 5 –Evaluate 6 - Create